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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,136	09/09/2004	William C. Moyer	SC12888TH	3949

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,136	MOYER ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

Status of Claims

Response to Amendment

Claims 1-23 were pending in this application. In response to the last Office Action, none of claims have been canceled, none of claims have been amended . As a result, claims 1-23 are remain pending in this application.

Claims 1-23 are rejected.

Applicant's arguments filed 12/14/05 have been fully considered with results as follows

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Macon Jr et al (US 5410653) as applied to claims 1,10 and 15 respectively and in view of Hussain et al (US 6901500).

As in claim 1, Macon describes data processing system (Fig 1), comprising: a first master (Fig 2: CPU); storage circuitry (Fig 2: #7 disk cache), coupled to the first master, for use by the first master; a first control storage circuit which stores a first prefetch limit (column 5 lines 45-66, length counter stores, Lmax, maximum number of prefetching blocks); a prefetch buffer (Fig 2: #7); and prefetch circuitry, coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry, said prefetch circuitry selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer (Fig 2: prefetching control circuits), wherein the first prefetch limit controls how many prefetches occur between misses in the prefetch buffer (Fig 6, Lmax column 5 lines 45-65 Lmax, maximum number of prefetching blocks). Macon does not specifically describe claim's detail of the master of the request. However, Hussain describes a memory system controller with multiple stream buffers, each stream has associating control circuit to control transferring data from memory to multiple processors" masters" (Fig 1; Fig 2, column 11, lines 20-40). It would have been obvious to one of ordinary skill in the art at the time of invention to include stream buffers and associating control circuits as suggested by Hussain in Macon's system to allow multiple requests being executed in a concurrently manner and thereby further optimizing the data transfer rate between processors "master" and main memory (Hussain's column 11 line 50 to column 12 line 10).

As in claim 2, Macon describes a counter to count the number of lines being read out from memory system (column 5 lines 45-66, Fig 3 length counter #16, #18).

As in claim 3, it is rejected based on the same rational as in claim 1. Macon does not specifically describe claim's detail of second control storage circuit. However, Hussain describes

a memory system controller with multiple stream buffers, each stream has associating control circuit to control transferring data from memory to multiple processors.

As in claim 4, it's rejected based on the same rationale as in claims 1 and 3.

As in claim 5, it's rejected based on the same rationale as in claims 2 and 3. Macon further describes the prefeching circuitry in column 5.

As in claim 6, the claim recites wherein the prefetch circuitry: selectively prefetches the predetermined number of lines for the first master based on the first prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the first master (Fig 6: #G hit prefetching; #N miss prefetching;). The second prefetching circuits are rejected based on the same rationale as in the rejection of claim 3.

As in claim 7, it is rejected based on the same rationale as in claim 6.

As in claim 8, Macon describes wherein the first control storage circuit is programmable (Macon's column 7 lines 25-38 describes the counter prefetching limit value can be dynamically loaded to have other values).

As in claim 9, Macon describes comprising a request monitor coupled to the first control storage circuitry, wherein the request monitor selectively updates the prefetch limit based on a number of buffer hits in the prefetch buffer accessed between two misses in the prefetch buffer. (Fig 6: #D, the counter value is updated when request hit in the prefetched buffer; #L and #N shows the fetching of buffer miss requests).

As in claim 10, the claim recites receiving a plurality of access requests from a master to access storage circuitry; and using a prefetch limit to limit a number of prefetches performed

between misses in a prefetching buffer resulting from at least a portion of the plurality of access request. The claim rejected based on the same rationale as in the rejection of claims 3 and 9.

Claim 11 rejected based on the same rationale as in claim 1.

As in claim 12, Macon describes counting prefetches after miss in the prefetch buffer to determine when the prefetch limit is reached (Macon's column 5 lines 10-40).

As for claim 13, Macon describes wherein each prefetch prefetches a single line from the storage circuitry (Macon's column 7 lines 15-26,Lmin value can be any values, for example one).

As for claim 14, the claim recites each single line prefetch is peformed in response to at least one of a hit or miss in the prefetch buffer. The claim rejected based on the same rationale as in the rejection of claims 7,13.

As in claim 15, the rejected based on the same rationale as in claim 1. Macon further shows in case of a buffer hit, performing prefetching next data blocks; Fig 6: #G and in case of a buffer miss performing the demand fetch and the next data block; data block length value is decremented; Fig 6: #N; column 7 lines 1-12.

As in claim 16, the claim recites wherein selectively performing the prefetch of the predetermined number of lines is further based on whether or not the predetermined number of lines is already present in the prefetch buffer. Macon's Fig 6 describes the prefetching operation is based on whether an amount of data blocks have been prefetched (Macon's column 9 lines 20-30).

As in claim 17, it's rejected based on the same rationale as in the rejection of claim 16.

As in claim 18, the claim recites wherein the second value corresponds to a prefetch limit and wherein updating the counter comprises decrementing the prefetch counter. Macon's Fig 6: #M describes the length counter value is being decremented for a miss buffer case.

As in claims 19-20, the claims recite wherein the first value corresponds to a prefetch limit and wherein updating the counter comprises incrementing the prefetch counter (claim 19); not prefetching from the storage circuitry when the read request results in a hit and the prefetch counter has reach the first value (claim 20). Macon describes in Fig 6 when a hit occurs in the prefetch buffer, the value of the length counter will be "updated" by incrementing its prefetching value; Fig 5: #E; Subsequently, the value of the counter is then used to fetch L data blocks as shown in Fig 6: #G. Thus Macon clearly suggests the counter is used to count the data blocks being fetched from memory and therefore the prefetching activity will stop when it reaches its values.

As in claims 21, the claim recites prefetching a predetermined number of lines from the storage circuitry when the read request results in a miss. The claim rejected based on the same rationale as in the rejection of claim 7.

As in claim 22, the claim recites herein selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value is performed such that the predetermined number of lines comprises only a single line. The claim rejected based on the same rationale as in the rejection of claim 13.

As in claim 23, the claim recites receiving a master identifier corresponding to the master, and selecting the prefetch counter from a plurality of prefetch counters based on the

master identifier. Macon describes the technique can be used in a multi-processor data processing system, Macon's column 4, lines 40-48; Macon further teaches the prefetching method is based on requests being assigned to I/O processes, Thus, these requests must have the associating ID's to identify them to the controller so that the prefetching data can be returned by the controller to the proper requesters.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
2/13/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER